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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,790	07/24/2003	James Y. Cho	5580-01302	1212

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EXAMINER	
NGUYEN, HIEP T	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/626,790	CHO ET AL.	
	Examiner	Art Unit	
	Hiep T Nguyen	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *65-90* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *65-90* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/24/03 & 5/28/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is a response to the preliminary amendment filed April 8, 2004. Newly added claims 65-90 are pending in the application. Applicant has canceled claims 1-64.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 65-66 and 78-79 are rejected under 35 U.S.C. 102(b) as being anticipated by Jeddeloh, U.S. Patent No. 6,049,855.

   (a) As per claim 65: Jeddeloh teaches a memory controller [figure 5] comprising:

      i. A first channel control circuit (16) configured to coupled to a first channel to access a first memory section (12);

      ii. A second channel control circuit (18) configured to couple to a second channel to access a second memory section (14), wherein the second channel is independent of and separate from the first channel; and

      iii. One or more registers (100, 102) programmable with a first indication of whether or not the first and the second channel are interleaved [col. 8, lines 35-45].

   (b) As per claim 66: Jeddeloh further teaches that the first the first indication identifies which portion of an address received by the memory controller is used to select between the first and second channel if the first and second channel are interleaved [col. 5, line 58 through col. 6, line 5; col. 6, lines 32-52].

   (c) As per claims 78 and 79: the claimed system comprises no more than the memory controller as claimed in claims 65 and 66 with an exception of the further claimed limitation of the processor configured to transmit an address of a memory location to be

accessed. Jeddeloh further tech such processor through the processors (22, 24); see figure 1]. Accordingly, Jeddeloh further anticipates the system of claims 78 and 79.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 67-77 and 80-90are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh, as applied to claims 65 and 78, above, and further in view of well-known features of which Official Notice is hereby taken.

   (a) As per claim 67:

      i. Jeddeloh teaches a memory controller as mentioned in the rejection of claim 65.

      ii. Jeddeloh, however, does not teaches a more than two channel control circuits that including the first and second channel control circuits, and that the first indication further indicates whether or not other ones of the plurality channel control circuits are interleaved.

      iii. A memory controller having more than two control channels and that more than two way interleave have also been known and widely implemented in the pertinent art. Obviously, the more memory controller channels are utilized, the higher bandwidth the system would get since the channels can access the coupled memory sections in parallel.

      iv. Accordingly, it would have been obvious to one having ordinary skill in the pertinent art at the time the invention was made to employ more than two controller channels in to that of the Jeddeloh memory controller and further

configure/program the Jeddeloh configuration registers in indicates whether or not the controller channels other than the first and second channels are interleaved. The ability to further improved he system bandwidth provides sufficient suggestion and motivation to one having ordinary skill in the pertinent art to do such further channels adding and configuration registers programming in the Jeddeloh system.

(b) As per claims 68 and 75: similarly to claim 67, employing a plurality memory chips within a memory modules such as that of Jeddeloh memory modules (12, 14) has also been known and widely used in the pertinent art. Obviously, when more than one memory chip is being used in a memory modules, more than one chip select would be used to select the corresponding memory chips. Accordingly, it would have been obvious to one having ordinary skill in the pertinent art to employ a plurality memory chips in each of the Jeddeloh memory modules (12, 14) and provide a corresponding memory chip select signal to each chip, if such features are not already inherent in the Jeddeloh system.

(c) As per claims 69-74 and 76-77, the further claimed limitations of interleaved subsections, no interleave, or different interleave mode for different memory subsections are directly taught by Jeddeloh [see figures 5 and 6].

(d) As per claims 80-90: the claimed system comprises no more than the memory controller as claimed in claims 67-77 with an exception of the further claimed limitation of the processor configured to transmit an address of a memory location to be accessed. Jeddeloh further tech such processor through the processors (22, 24); see figure 1]. Accordingly, Jeddeloh further anticipates the system of claims 80-90.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep T Nguyen whose telephone number is (703) 305-3822. The examiner can normally be reached on Monday-Friday from 9:30 a.m. to 6:00 p.m.

7. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (703) 308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.
8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep T Nguyen
Primary Examiner
Art Unit 2187

HTN